# HS2303

## 10A, High Efficiency Power Module

### FEATURES:

- High Power Density Power Module
- 10A Maximum Load
- Input Voltage Range from 4.5V to 24V
- VCC Voltage Range from 4.5V to 13.2V
- Output Voltage Range from 1V to 6V
- Excellent Thermal Performance
- 96% Peak Efficiency
- Enable Function
- Protections (OVP, UVP, UVLO, OCP)
- Power Good Indicator
- Internal Soft Start with Pre-bias Output Start-Up
- Fast Transient Response
- QFN-Stack Package 12mm*12mm*6.0mm
- Pb-free Available (RoHS compliant)
- MSL 3, 245C Reflow

### APPLICATIONS:

- General Buck DC/DC Conversion
- Distributed Power Supply
- Datacom, and Telecom Power Supplies
- Server/Desktop Power Supplies
- LDOs Replacement
- Cell Phones / PDAs / Palmtops

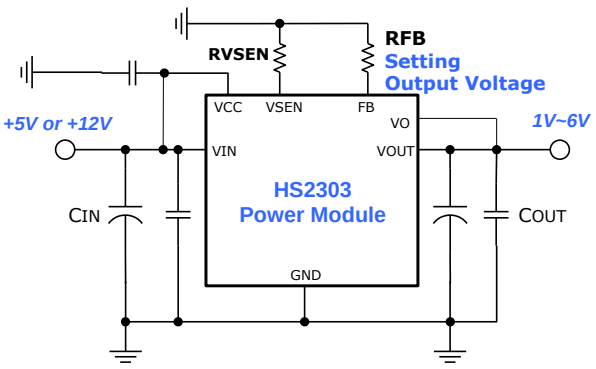
### GENERAL DESCRIPTION:

The HS2303 is a high frequency, high power density and complete DC/DC power module. The PWM controller, power MOSFETs and most of support components are integrated in one hybrid package. Additional, a new patent technology is adopted to stack power choke on the hybrid module in order to achieve high power density.

The features of HS2303 include voltage mode control with high phase margin compensation, internal soft-start, protections and pre-biased output start-up capability. Besides, HS2303 is an easy to use DC/DC power module, only input capacitors and output capacitors need to design for all kinds of applications.

The compact package enables utilization of unused space on the bottom of PC boards for needing high density space applications. The HS2303 is packaged in a thermally enhanced, compact (12mm*12mm*6mm) and low profile QFN package suitable for automated assembly by standard surface mount equipment. The HS2303 is Pb-free and RoHS compliance.

### TYPICAL APPLICATION CIRCUIT & PACKAGE:



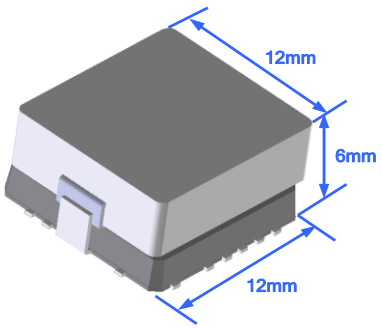




TABLE 1: OUTPUT VOLTAGE SETTING

| Vout | 1.0V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | 5V |
|---|---|---|---|---|---|---|---|
| RFB (Ohm) | 8.87k | 4.42k | 2.55k | 1.74k | 1.02k | 0.715k | 0.412k |

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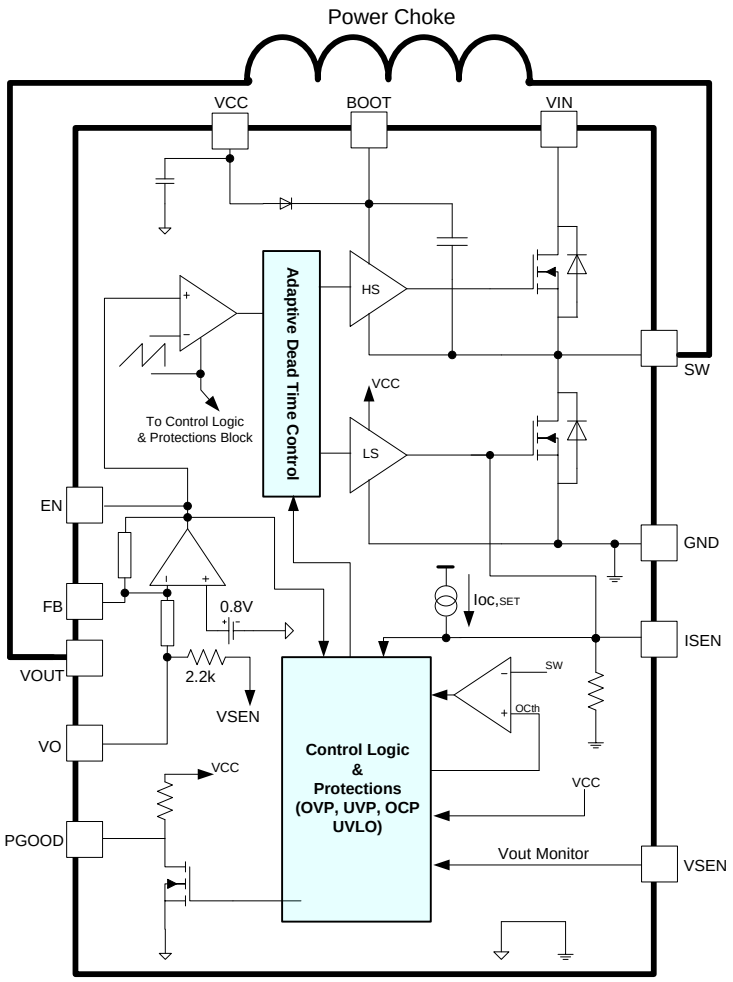
## 10A, High Efficiency Power Module

### ORDER INFORMATION:

| Part Number | Temp. Range (°C) | Package (Pb-Free) | MSL | Note |
|---|---|---|---|---|
| HS2303 | -40 ~ 85 | Stack-QFN | Level 3 | - |

| Order Code | Packing | Quantity |
|---|---|---|
| HS2303 | Tray | 90 |
| HS2303-T | Tape and reel | 400 |

### SIMPLIFIED INTERNAL BLOCK DIAGRAM:

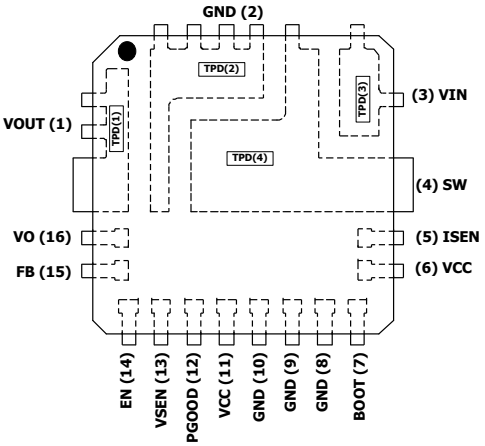



***DC/DC Power Module***

# HS2303

## 10A, High Efficiency Power Module

### PIN CONFIGURATION:




### PIN DESCRIPTION:

| Name | No. | I/O | Description |
|---|---|---|---|
| VOUT | 1 | O | Output voltage from the module. Output voltage range:1V to 6V |
| VO | 16 | I | Output voltage sensing pin. |
| GND | 2, 8~10 | -- | All voltage levels are referenced to the pins. All pins should be connected together with a ground plane |
| VIN | 3 | I | Analog Voltage Input. When the pin directly connects to VCC pin whose range is from 4.5V to 13.2V. |
| SW | 4 | O | The pin is phase node of the DC/DC module. |
| BOOT | 7 | I | Gate driver voltage for internal control N-type MOSFET |
| ISEN | 5 | O | The ISEN pin is over current protection setting. It compares the $R_{DS(ON)}$ of low-side MOSFET to configure the over current protection trip current. The HS2303 has initial current setting to limit the surge current impact. It has an integrated internal 17.8kΩ resistor ($R_{SEN-IN}$) between ISEN and PGND pin. One can also connect external resistor ($R_{SEN-EX}$) between this pin and PGND pin to reduce the over current trip point. The recommendation of this external resistor ($R_{SEN-EX}$) is 75kΩ for general application limit .Place this resistor as closely as possible to this pin. |

## PIN DESCRIPTION: (Cont.):

| | | | |
|---|---|---|---|
| VCC | 6, 11 | I | Power input for supplying internal PWM controller and for driving internal control and synch. MOSFETs. |
| PGOOD | 12 | O | Open drain power output voltage. |
| VSEN | 13 | O | Regulated voltage sense pin for OVP and UVP protections and PGOOD. |
| EN | 14 | O | Disable – to pull the pin lower than 0.75V (typ.)<br>Enable – to float the pin |
| FB | 15 | I | Internal EA inversing input. |

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## 10A, High Efficiency Power Module

### ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| ■ Absolute Maximum Ratings | | | | | |
| VCC to GND | | PGND-0.3 | - | +15 | V |
| BOOT to GND | | PGND-0.3 | - | +33 | V |
| BOOT to SW | | - | - | +15 | V |
| VIN to SW | Note 1 | -1.2 | - | +30 | V |
| SW to GND | Note 1 | -1.2 | - | +30 | V |
| ISEN to GND | | PGND-0.3 | - | VCC+0.3 | V |
| PGOOD to GND | | PGND-0.3 | - | VCC+0.3 | V |
| VSEN, EN, FB to GND | | PGND-0.3 | - | +3.6 | V |
| VO to GND | | - | - | +5.5 | V |
| Tc | | - | - | +125 | °C |
| Tj | | -40 | - | +125 | °C |
| Tstg | | -40 | - | +125 | °C |
| ESD Rating | Human Body Model (HBM) | 2000 | - | - | V |
| | Machine Model (MM) | - | - | 100 | V |
| | Charge Device Model (CDM) | - | - | 1000 | V |
| ■ Recommendation Operating Ratings | | | | | |
| VIN | Input Supply Voltage | +4.5 | - | +24 | V |
| VOUT | Output Voltage | +1.0 | - | +6.0 | V |
| VCC | Fixed Supply Voltage for 5V | +4.5 | +5 | +5.5 | V |
| | Fixed Supply Voltage for 12V | +10.8 | +12 | +13.2 | V |
| | Wide Range Supply Voltage | +4.5 | - | +13.2 | V |
| Ta | Ambient Temperature | -40 | - | +85 | °C |
| ■ Thermal Information | | | | | |
| Rth(j-a) | Thermal resistance from junction to ambient. (Note 2) | - | 17.8 | - | °C/W |

NOTES:
1. $V_{DS}$ (Drain to Source) specification for internal high-side and low-side MOSFETs.
2. Rth(j-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition.

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## 10A, High Efficiency Power Module

### ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: $T_A$ = 25 ºC, Vin = 12V, Vout = 3.3V, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ■ Input Characteristics | | | | | | |
| $I_{Q(IN)}$ | Input supply bias current | Vin = 12V, Iout = 0A<br>EN = VIN<br>Vout = 3.3V | - | 0.25 | - | mA |
| $I_{S(IN)}$ | Input supply current | Vin =12V, EN = VIN | - | - | - | - |
| | | Iout = 1mA<br>Vout = 3.3V | - | 0.6 | - | mA |
| | | Iout = 100mA<br>Vout = 3.3V | - | 33 | - | mA |
| | | Iout = 1000mA<br>Vout = 3.3V | - | 320 | - | mA |
| ■ Output Characteristics | | | | | | |
| $I_{OUT(DC)}$ | Output continuous current range | Vin=12V, Vout=3.3V | 0 | - | 1000 | mA |
| $V_{O(SET)}$ | Ouput voltage set point | With 0.5% tolerance for external resistor used to set output voltage | -3.0 | | +3.0 | % $V_{O(SET)}$ |
| $\Delta V_{OUT}$ /$\Delta V_{IN}$ | Line regulation accuracy | Vin = 5V to 12V<br>Vout = 3.3V, Iout = 0A<br>Vout = 3.3V, Iout = 1000mA | - | 0.1 | 0.2 | % $V_{O(SET)}$ |
| $\Delta V_{OUT}$ /$\Delta I_{OUT}$ | Load regulation accuracy | Iout = 0A to 1000mA<br>Vin = 12V, Vout = 3.3V | - | 0.5 | 1.0 | % $V_{O(SET)}$ |
| $V_{OUT(AC)}$ | Output ripple voltage | Vin = 12V, Vout = 3.3V<br>EN = VIN | - | | - | - |
| | | Iout = 1mA | | 14 | | mVp-p |
| | | Iout = 1000mA | | 8 | | mVp-p |

# HS2303

## 10A, High Efficiency Power Module

### ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: TA = 25 ºC, unless otherwise specified. Vin=12V, Vout=1.5V, Cin=22uF/Ceramic×3, Cout=100uF/Ceramic×3

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ■ Control Characteristics | | | | | | |
| $V_{REF}$ | Referance voltage | TA = 25 ºC | 0.792 | 0.8 | 0.808 | V |
| | | -40 ºC ≦ TA ≦ 60 ºC | 0.788 | 0.8 | 0.812 | V |
| $F_{OSC}$ | Oscillator frequency | Note 3 | 540 | 600 | 660 | kHz |
| $R_{FB-TI}$ | Internal resistor between VOUT and FB pins | | 2.17 | 2.20 | 2.22 | kΩ |
| $V_{ENDIS}$ | Disable threshold voltage (EN) | Note 3 | 0.70 | 0.78 | 0.85 | V |
| $R_{PGOOD}$ | Internal resistor between VCC and PGOOD pins | | 21.78 | 22.00 | 22.22 | kΩ |
| $V_{PG-H}$ | PGOOD voltage High | PGOOD Open / No Fault | - | VCC | - | V |
| $V_{PG-L}$ | PGOOD voltage Low | PGOOD Open / Fault | - | - | 0.4 | V |
| $V_{PG-up}$ | PGOOD upper threshold voltage | VSEN rising, Note 3 | 0.86 | 0.89 | 0.92 | V |
| $V_{PG-low}$ | PGOOD lower threshold voltage | VSEN falling, Note 3 | 0.68 | 0.71 | 0.74 | V |
| ■ Fault Protection | | | | | | |
| $R_{SEN-IN}$ | Internal resistor between ISEN and PGND pins | | 17.62 | 17.8 | 17.98 | kΩ |
| $I_{OC,SEN}$ | IOC,SET current source | Note 3 | 9 | 10 | 11 | uA |
| $R_{VSEN-IN}$ | Internal resistor between VSEN and VO pins | | 2.17 | 2.20 | 2.22 | kΩ |
| OVP | Over voltage protection threshold | VSEN rising, Note 3 | 0.9 | 1.0 | 1.1 | V |
| | | Unlatch, VSEN, falling, Note 3 | 0.35 | 0.40 | 0.45 | V |
| UVP | Under voltage protection threshold | VSEN falling, Note 3 | 0.5 | 0.6 | 0.7 | V |

NOTES:

3. Parameters guaranteed by PWM IC vendor design and test prior to module assembly.

# HS2303

## 10A, High Efficiency Power Module

### TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: Ta=25 degree C. Input capacitors= 22uF/16V *5, X5R, Ceramic capacitors. Output capacitors=100uF/6.3V*6, X5R, Ceramic capacitors. ΔIout=10A and slew rate=2.5A/uSec for dynamic test VIN pin and VCC are connected together by 0 Ohm.

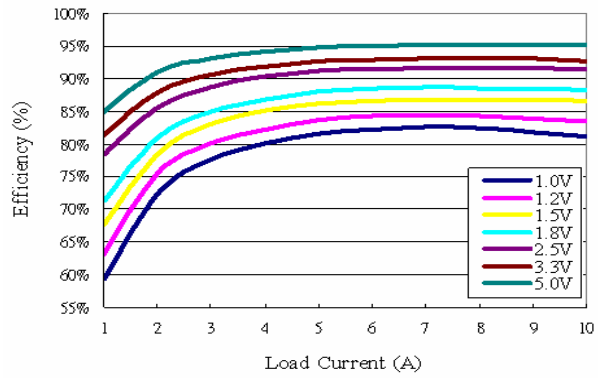



**Figure. 1. 12VIN, 12VCC Efficiency v.s Load Current**

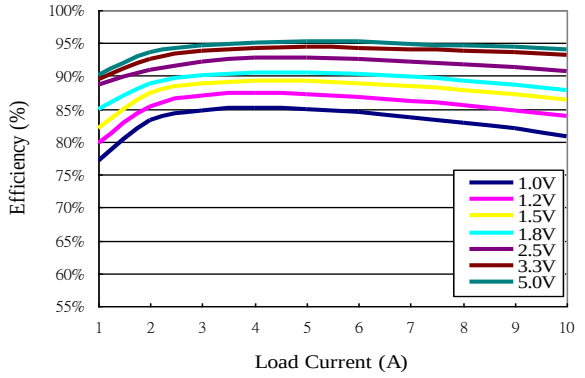



**Figure. 2. 12VIN, 5VCC Efficiency v.s Load Current**

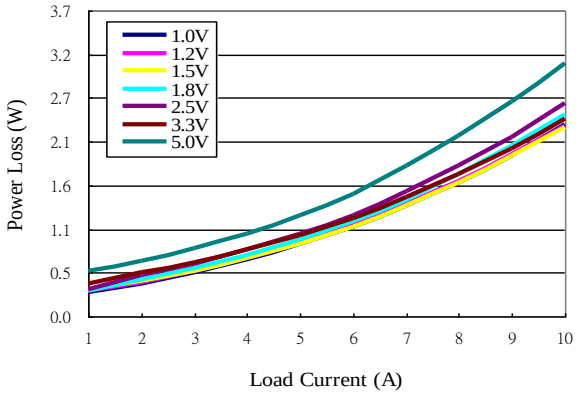



**Figure. 3 12VIN Power Loss v.s Load Current**

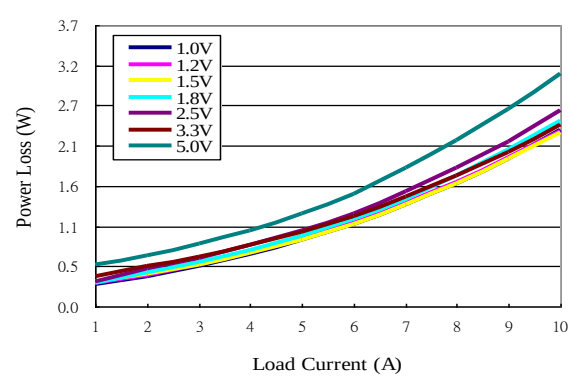



**Figure. 4. 12VIN, 5VCC Power Loss v.s Load Current**

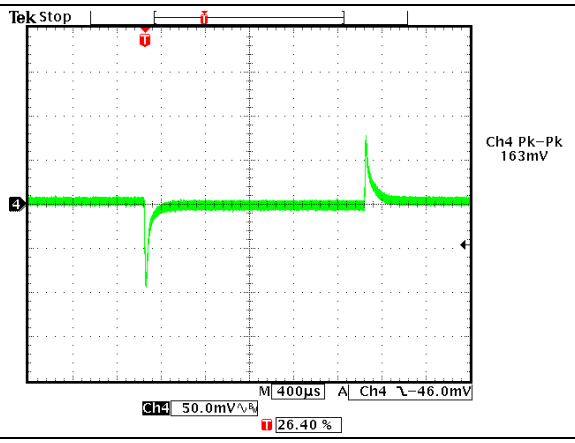



**Figure. 5 Load Transient Response, 12VIN/1.0VOUT**

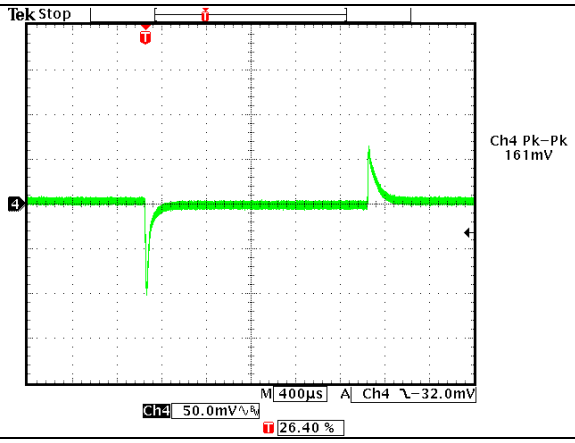



**Figure. 6 Load Transient Response, 12VIN/1.2VOUT**

# HS2303

## 10A, High Efficiency Power Module

### TYPICAL PERFORMANCE CHARACTERISTICS: (Cont.)

Conditions: Ta=25 degree C. Input capacitors= 22uF/16V *5, X5R, Ceramic capacitors. Output capacitors=100uF/6.3V*6, X5R, Ceramic capacitors. ΔIout=10A and slew rate=2.5A/uSec for dynamic test VIN pin and VCC are connected together by 0 Ohm.

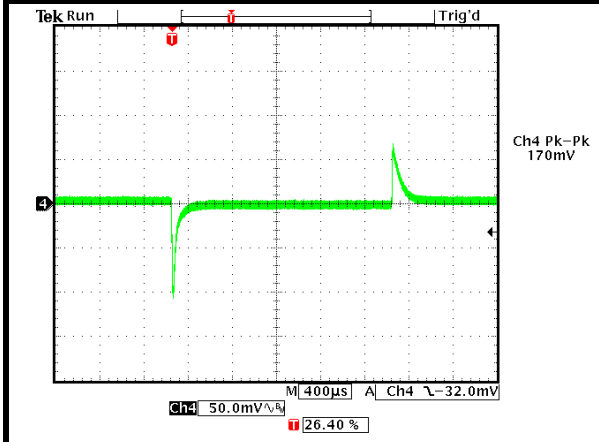



Figure. 7 Load Transient Response, 12VIN/1.5VOUT

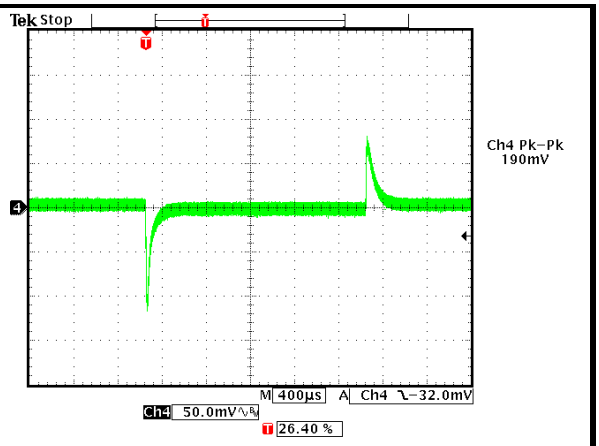



Figure. 8 Load Transient Response, 12VIN/2.5VOUT

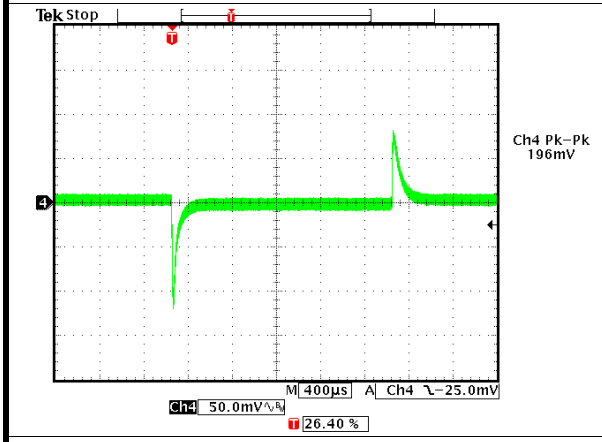



Figure. 9 Load Transient Response, 12VIN/3.3VOUT

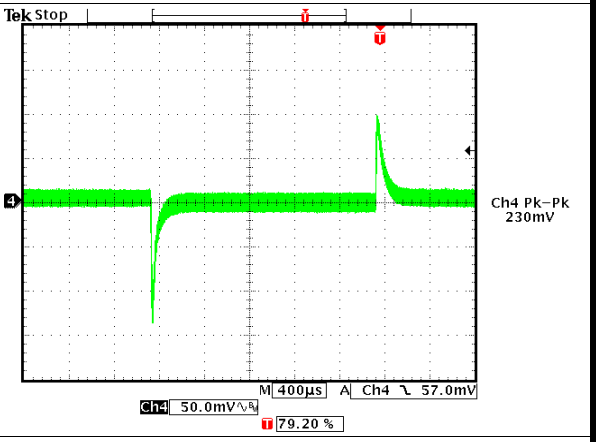



Figure. 10 Load Transient Response, 12VIN/5.0VOUT

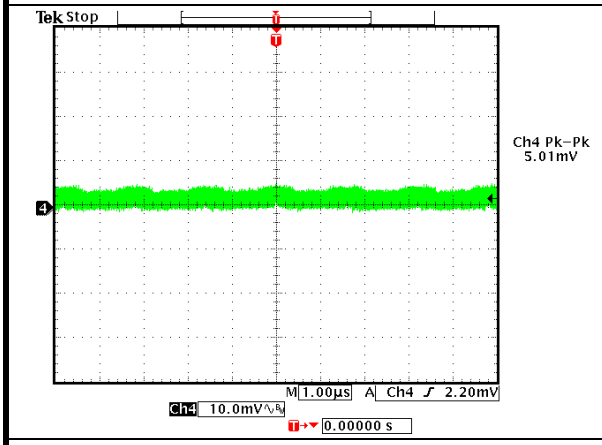



Figure. 11 Output Ripple Voltage, 12VIN/1.0VOUT

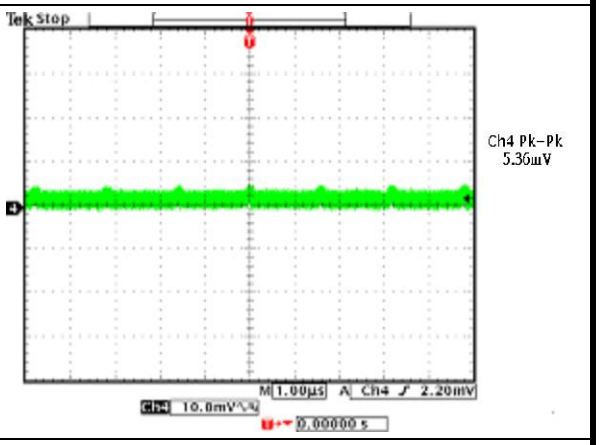



Figure. 12, Output Ripple Voltage, 12VIN/1.8VOUT

# HS2303

## 10A, High Efficiency Power Module

### TYPICAL PERFORMANCE CHARACTERISTICS: (Cont.)

Conditions: Ta=25 degree C. Input capacitors= 22uF/16V *5, X5R, Ceramic capacitors. Output capacitors=100uF/6.3V*6, X5R, Ceramic capacitors. ΔIout=10A and slew rate=2.5A/uSec for dynamic test VIN pin and VCC are connected together by 0 Ohm.

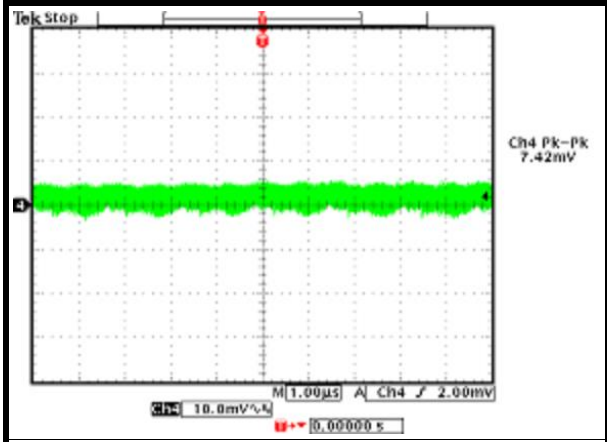



Figure. 13 Output Ripple Voltage, 12VIN/3.3VOUT

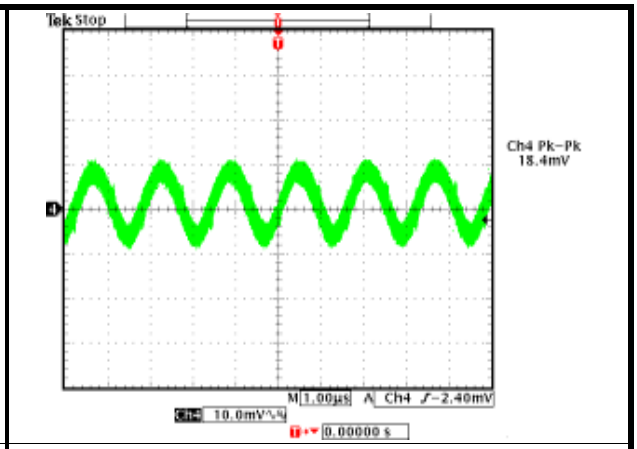



Figure. 14 Output Ripple Voltage, 12VIN/5.0VOUT

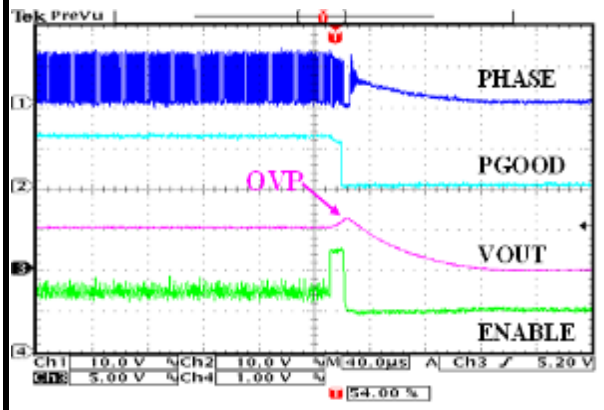



Figure. 15 Over-Voltage Protection

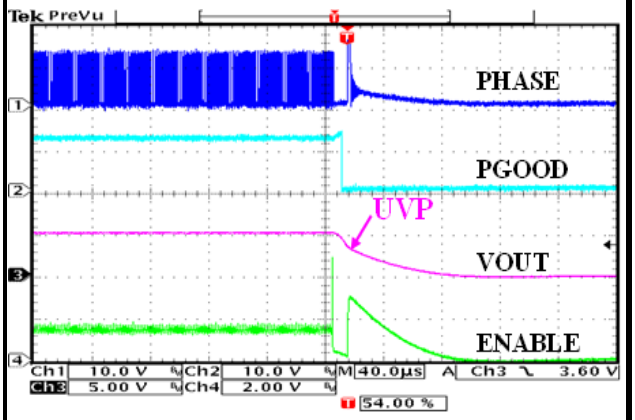



Figure. 16 Under-Voltage Protection

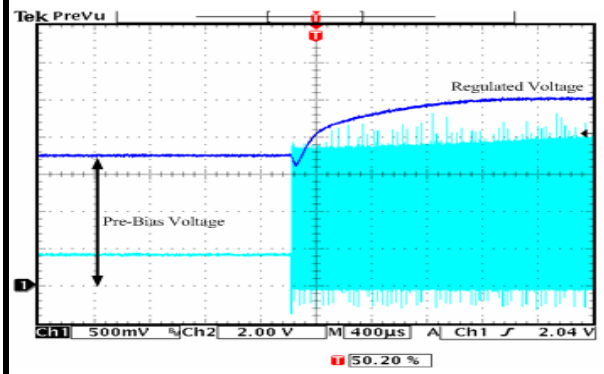



Figure. 17 Start-Up with Pre-Bias Voltage

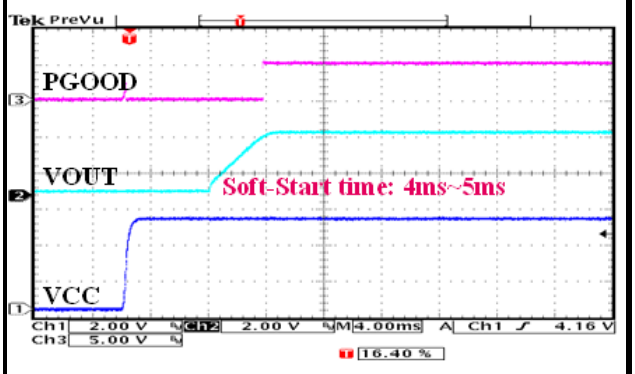



Figure. 18 Power Start-Up with No Load

# HS2303

## 10A, High Efficiency Power Module

### TYPICAL PERFORMANCE CHARACTERISTICS: (Cont.)

Conditions: Ta=25 degree C. Input capacitors= 22uF/16V *5, X5R, Ceramic capacitors. Output capacitors=100uF/6.3V*6, X5R, Ceramic capacitors. ΔIout=10A and slew rate=2.5A/uSec for dynamic test VIN pin and VCC are connected together by 0 Ohm.

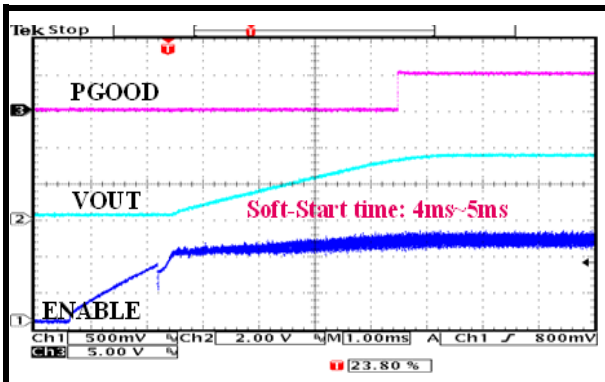



Figure. 19 Enable Start-Up with Full Load

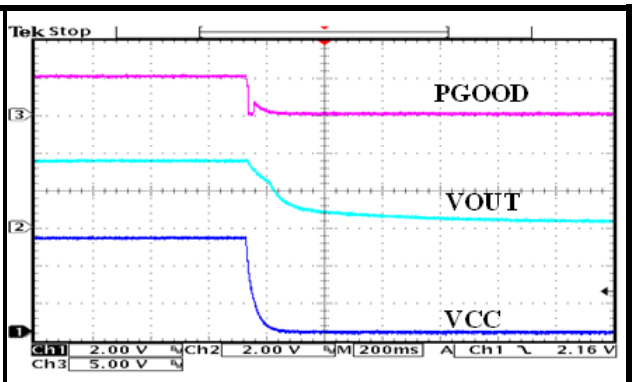



Figure. 20 Power Shunt-Down with No Load

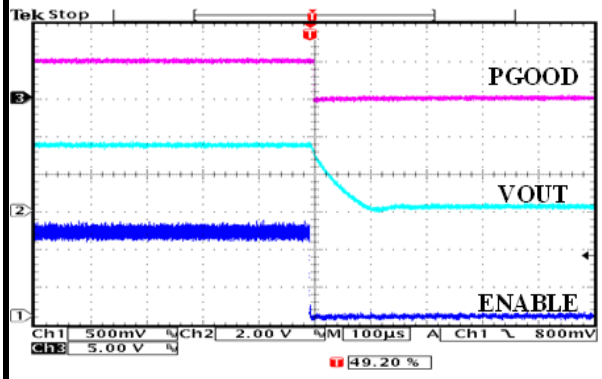



Figure. 21 Enable Shunt-Down with Full Load

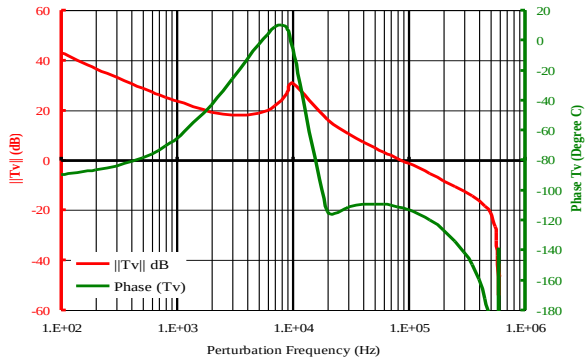



Figure. 22 Bode Plot (BW~75kHz, Phase Margin ~ 60°)

# HS2303

## 10A, High Efficiency Power Module

## THERMAL PERFORMANCE:

### Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 60mm×60mm×1.6mm with 4 layers, 2oz. The case temperature of module sensing point is shown as Figure 23. Then Rth(j-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The HS2303 module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature. The de-rating load current in different output voltage are shown in Figure 24, 25, 26, and 27. It would be convenient for user to confirm and estimate module's approximate performance according to actual operating conditions in beginning of design.

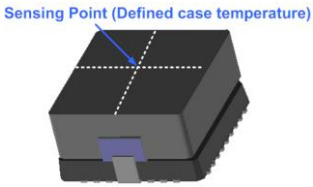



**Figure 23. Case Temperature Sensing Point**

**Thermal De-rating Curves:**

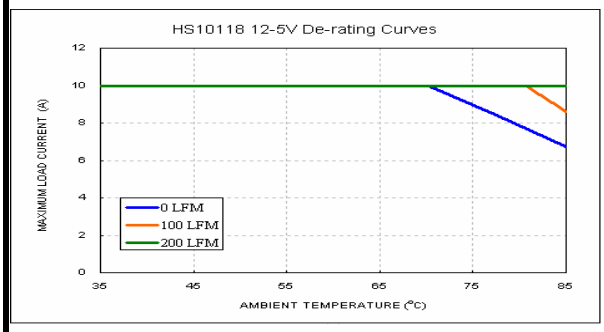



**Figure. 24 12VIN/5.0VOUT Thermal De-Rating Curves**

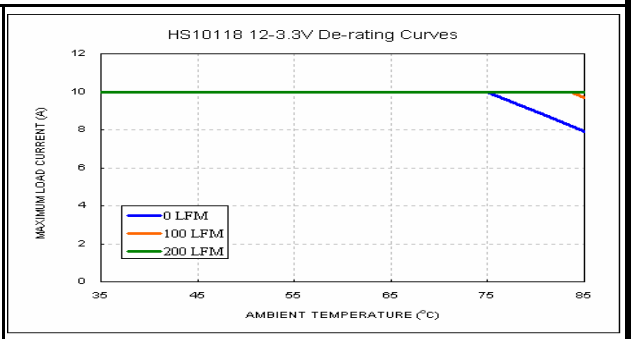



**Figure. 25 12VIN/3.3VOUT Thermal De-Rating Curves**

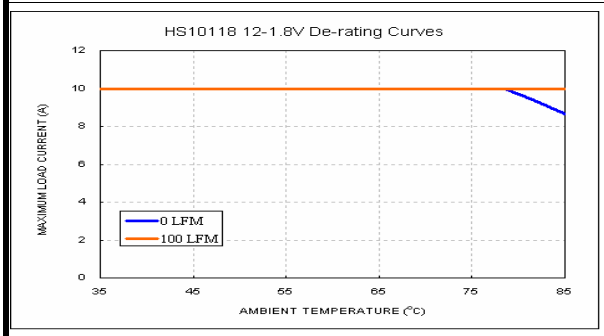



**Figure. 26 12VIN/1.8VOUT Thermal De-Rating Curves**

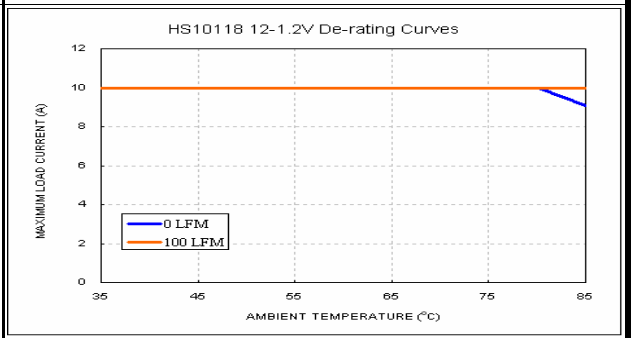



**Figure. 27 12VIN/1.2VOUT Thermal De-Rating Curves**

# HS2303

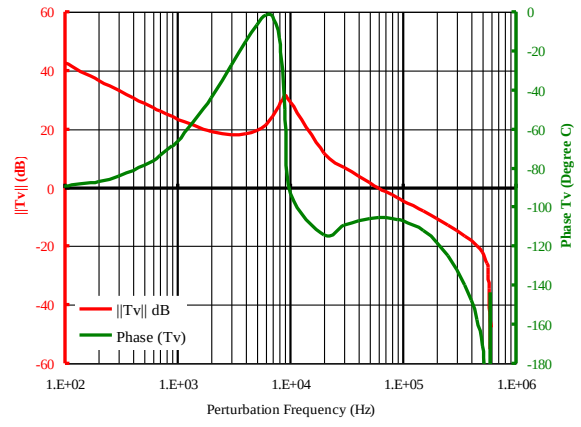
## 10A, High Efficiency Power Module

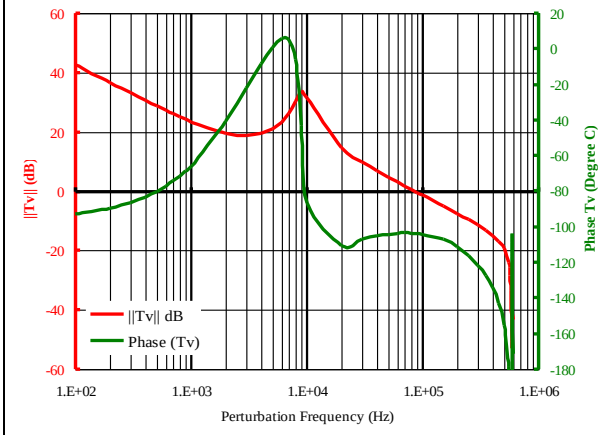
## APPLICATIONS INFORMATION:

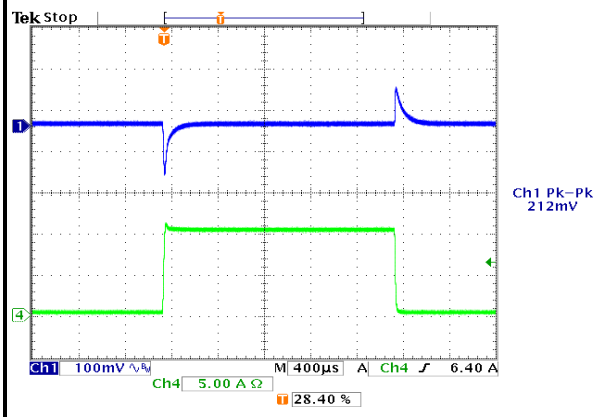
### 1. Fast Load Transient Response Design by Extending Bandwidth of Closed Loop System:

Adding an external ceramic capacitor from VOUT pin to FB pin can extend bandwidth of whole system so that the total output capacitance can be decreased. In other words, using this function can save both PCB space and total cost. Note that in order to avoid “side-band effect” of PWM modulator, the capacitance should not be larger than 4.7uF.

A design example: A typical design 12V/3.3V, ΔIout=10A and load slew rate=2.5uA/sec. With $C_{VF}$=0uF, 300uF output capacitance can suppress output voltage variation effectively, and the whole closed loop is keeping stable because of phase margin=65 degree C, as shown Figure 28. With $C_{VF}$=4.7uF, the smaller output voltage variation is quite obvious than the case CVF=0uF., as shown Figure. 29. Because of extending bandwidth from 55kHz to 85kHz. At the same time, the phase margin still keeps around 65 degree C for stability, as shown Figure. 29 right down.



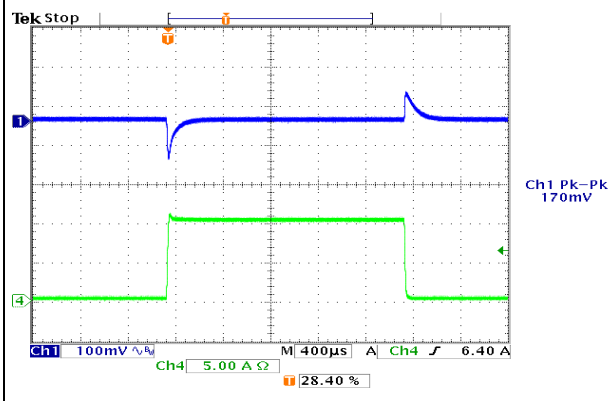




**Figure 28 Bandwidth=55kHz, Phase Margin=65 degree C, CVF=0uF**

**Figure 29 Bandwidth=80kHz, Phase Margin=65 degree C, CVF=4.7uF,**

## APPLICATIONS INFORMATION: (Cont.)

### 2. Output Voltage Setting

The output voltage setting resistor RFB needs to be connected from FB (13) pin to GND in order to set different output voltage. Output voltage can be adjusted by using following Equation 1.

$$V_{OUT} = 0.8 * (1 + \frac{2.2k}{R_{FB}}) (V) \quad \text{(EQ.1)}$$

Where, 0.8V is reference voltage (VREF) of positive input of internal error amplifier. Some typical output voltage setting resistance is shown as TABLE I on front cover page.

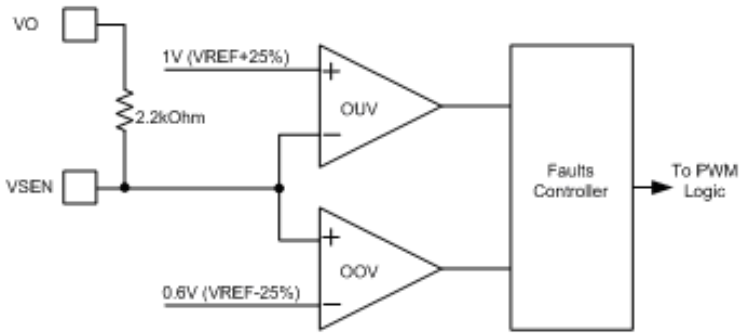
### 3. Output Over-Voltage (OOV)/Output Under-Voltage (OUV) Setting

**Output Over-Voltage Protection:** If the voltage at VSEN pin rises over OOV threshold (1 V typ), over-voltage protection turns off internal HS MOSFET and turns on LS MOSFET. The internal LS MOSFET will be turned off as soon as VSEN goes below VREF/2 (0.4 V). The condition is latched, cycle VCC to recover. Notice that, even if the device is latched, the device still controls the LS MOSFET and can switch it on whenever VSEN rises above 0.4 V.

**Output Under-Voltage Protection:** If the voltage at VSEN pin drops below OUV threshold, the device turns off both internal MOSFETs, latching the condition. Cycle VCC to recover.

After both the under-voltage and over-voltage events, normal operation can only be restored by cycling the VCC voltage.

**OOV/OUV Threshold Setting:** Connecting a resistor from VSEN pin to GND pin can be to set the OOV/OUV threshold. Usually, the resistance value is set to the same as the output voltage setting resistance RFB. Below figure shows the internal OOV/OUV protection circuit and its thresholds.



## APPLICATIONS INFORMATION: (Cont.)

### 4. Output Over-Current Setting

The over-current function protects the converter from a shorted output by using the low side MOSFET on-resistance, $R_{DS(ON)}$, to monitor the current. A resistor ($R_{SEN}$) programs the over-current trip level. This method reduces cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors. If over-current is detected, the output immediately shuts off. The over-current function will trip at a peak inductor current ($I_{PEAK}$) determined by Equation 2.

$$I_{PEAK} = \frac{1.5 \times I_{SEN} \times R_{SEN}}{R_{DS(ON)}} \quad \text{(EQ.2)}$$

Where:

$R_{DS(ON)}$ is typically 7.91mΩ including internal parasitic resistance. (at PVCC=$V_{GS}$=12V, $I_{DS}$=30A)

$R_{DS(ON)}$ is typically 9.84mΩ including internal parasitic resistance. (at PVCC=$V_{GS}$=5V, $I_{DS}$=30A)

$Ioc_{SEN}$ is the internal current source (10uA typ.)

$R_{SEN}$ is equivalent resistance between ISEN and PGND pins. The HS2303 has integrated 17.8kΩ resistance ($R_{SEN-IN}$). Therefore, the equivalent resistance of $R_{SEN}$ can be expressed in Equation 3.

$$R_{SEN} = \frac{R_{SEN-EX} \times R_{SEN-IN}}{R_{SEN-EX} + R_{SEN-IN}} \quad \text{(EQ.3)}$$

The relationships between the external $R_{SEN-EX}$ values and typical over current protection trip level of HS2303 are shown as TABLE 2.

TABLE 2 RECOMMENDATION OCP TRIP FOR $R_{SEN-EX}$ VALUES

| $R_{SEN-EX}$ | OCP Trip Level (Typ.) (Note 4)<br>VIN=12V, PVCC=12V, VOUT=5V | OCP Trip Level (Typ.) (Note 4)<br>VIN=12V, PVCC=5V, VOUT=5V |
|---|---|---|
| OPEN | CAUTION: Do not leave ISEN pin open | 25A |
| 75kΩ | 25A | 20A |
| 34kΩ | 20A | 16A |
| 21kΩ | 16A | 13A |
| 14kΩ | 13A | 10A |

NOTES:
4. The trip values are tested at $T_A$ = 25 ºC, Cin=22uF/Ceramic×5, Cout=100uF/Ceramic×6.
Test Board Information:60mm×60mm×1.6mm, 4 layers, 2oz.

## APPLICATIONS INFORMATION: (Cont.)

### 5. PGOOD

If the voltage monitored through VSEN exits from the PGOOD window limits, the device de-asserts the PGOOD signal still continuing switching and regulating. PGOOD is asserted at the end of the soft-start phase as shown in Figure 30.

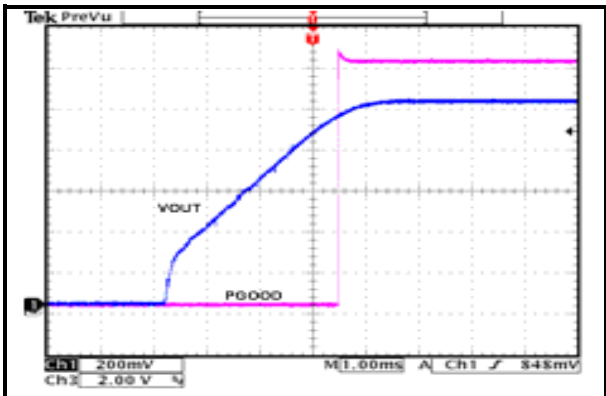



**Figure. 30 PGOOD with Start-Up Phase**

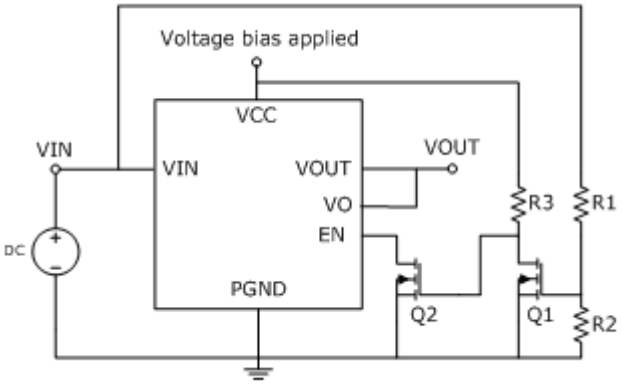
### 6. Enable/Disable

Pull EN pin (PIN14) to be lower than 0.75V can shut down the module and can float this pin enable the module again.

### 7. VCC Bias and Power-Up Sequence Considerations:

If VCC powers up faster than VIN which is not present by the time the initialization is done, then the soft-start will not be able to ramp the output, and the output will later follow part of the VIN ramp when it is applied. If this is not desired, then change the sequencing of the supplies, or use the EN pin to disable VOUT until both supplies are ready. The following figure shows a simple sequencer for this situation.

## APPLICATIONS INFORMATION: (Cont.)




### 8. Start-Up with Pre-Bias

In order to prevent any potential negative spike on VOUT during start-up, internal pre-bias function will perform a special H/S gate signal and L/S gate signal warm-up sequence. HS2303 performs a special sequence in enabling LS driver to switch: during the soft-start phase, the LS driver results disabled (LS = OFF) until the HS starts to switch. In order to avoid the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output. Figure 19 shows that VOUT rise from its initial value and no larger negative undershoot will happen.

### 9. Safety Considerations

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations.

For safety agency approvals, install the converter in compliance with the end-user safety standard.

## APPLICATIONS INFORMATION: (Cont.)

### 10. Recommended PCB Layout

Some layout considerations are necessary for achieving noise-less, low loss and good thermal performance.

1. Place high frequency ceramic capacitor (at least 10uF) between VIN terminal and GND pad must as close as possible for reducing high frequency noise. Note: the placement of the input capacitor is very critical.
2. Use large copper areas for power path (VIN, GND and VOUT) to reduce parasitic effect (resistance and inductance) and to increase thermal sink capability. Also, use multiple vias to connect the power planes in different layers for enhancing thermal performance of the power module.
3. Control signals (FB, VSEN..), keep the trace to set resistors (RFB, RVSEN) as short as possible
4. Sensitive signal (FB, VSEN, EN) trace need to avoid closing the noise signal such as SW node, BOOT pin and ISEN pin.

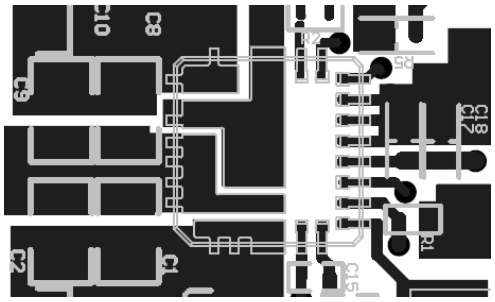
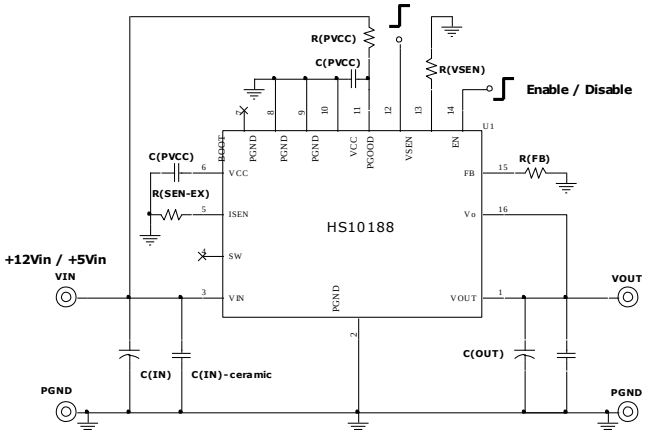



**Figure 31 Recommend PCB Layout**

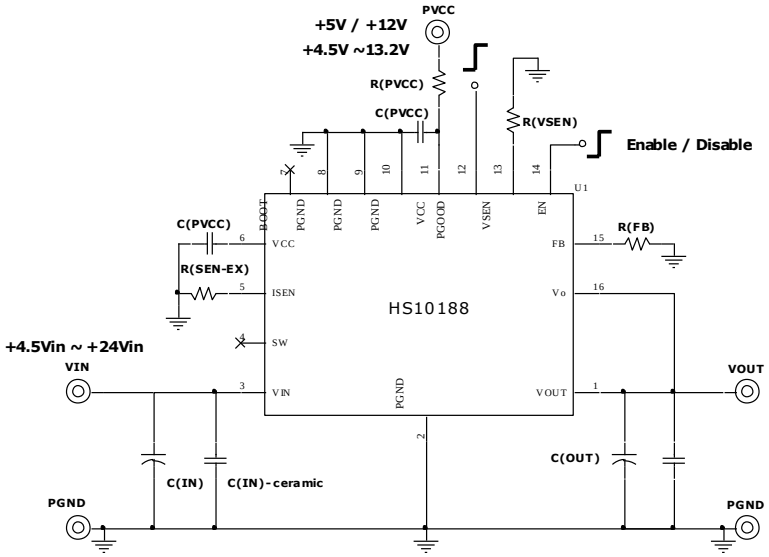
### 11. Reference Circuits for General Applications:

The figure shows the HS2303 application schematics for input voltage +5V or +12V. The VCC pin can connect to input supply through a RC filter.



## APPLICATIONS INFORMATION: (Cont.)

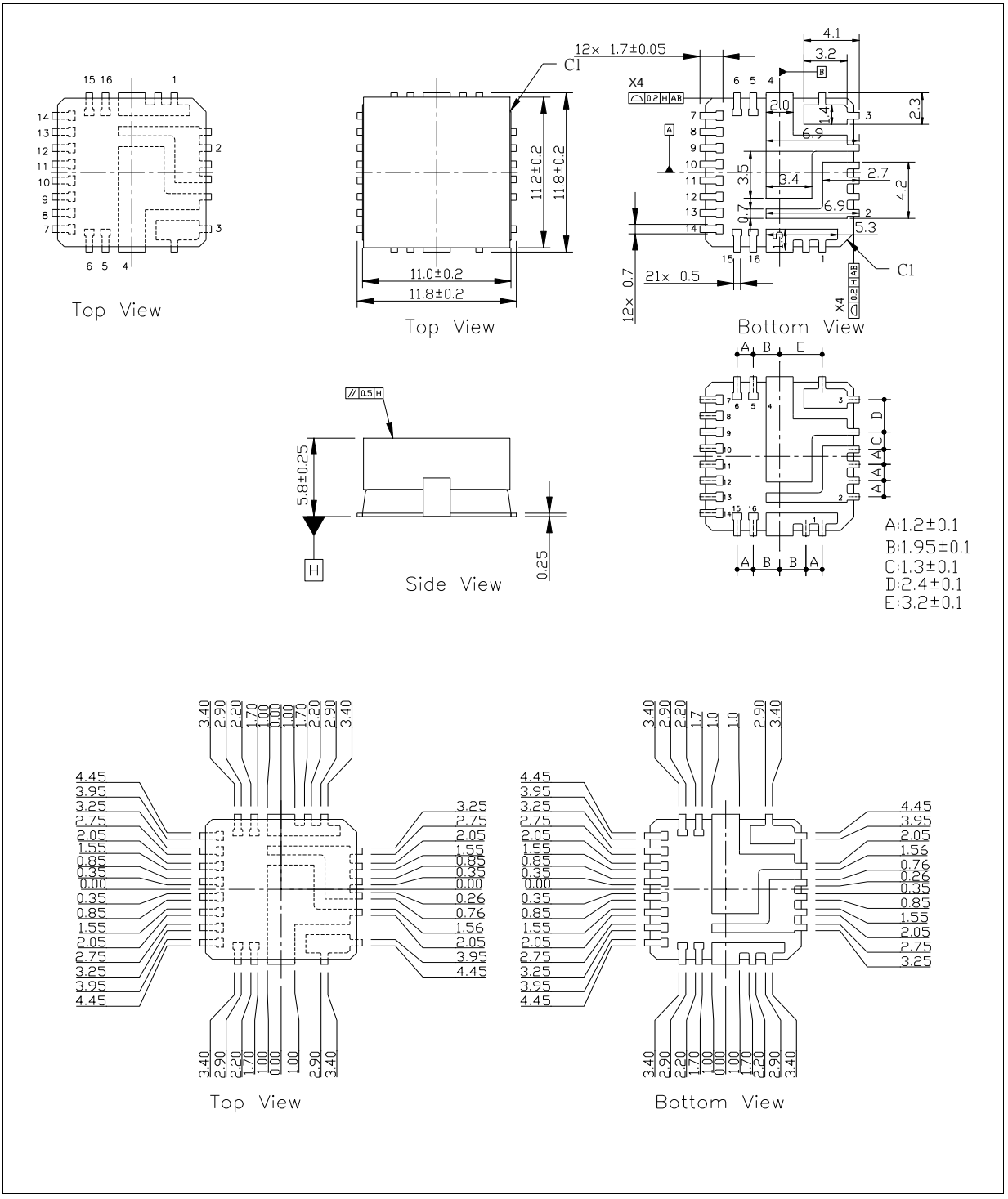
Another figure shows the HS2303 application schematics for wide input voltage from +1V to +24V. The VCC supply can be optimum for decreasing driver loss, the smaller driver voltage (VCC) can improve efficiency of light load. Please refer to input voltage consideration in application information.



# HS2303

## 10A, High Efficiency Power Module

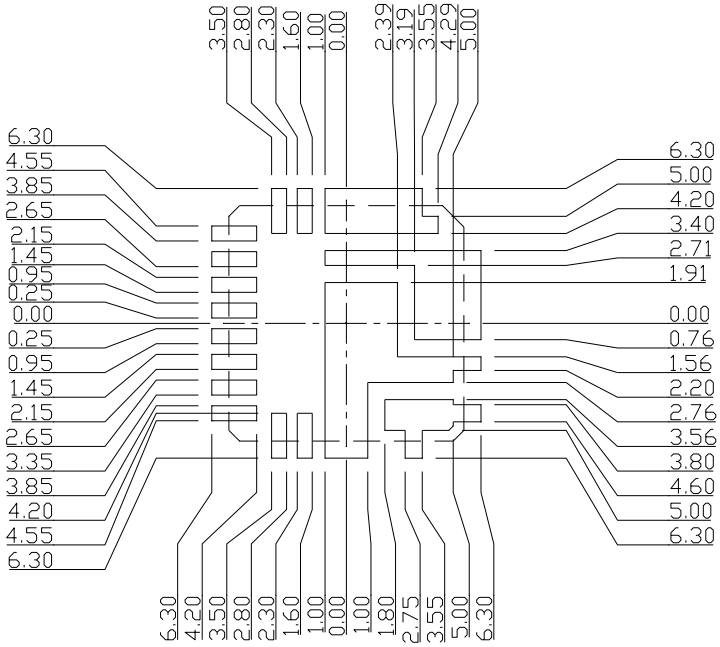
### PACKAGE OUTLINE DRAWING:



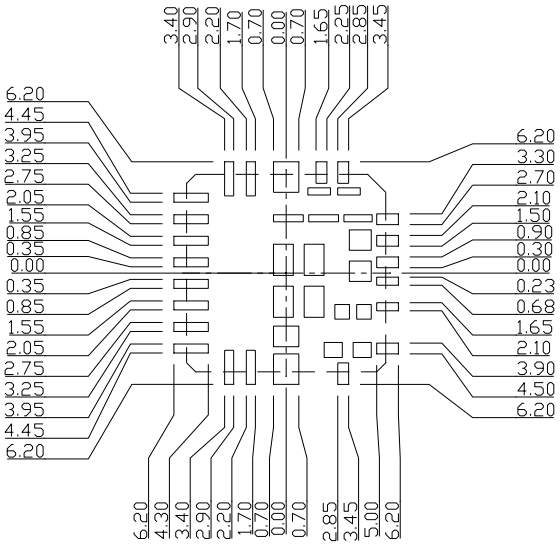
# HS2303

## 10A, High Efficiency Power Module

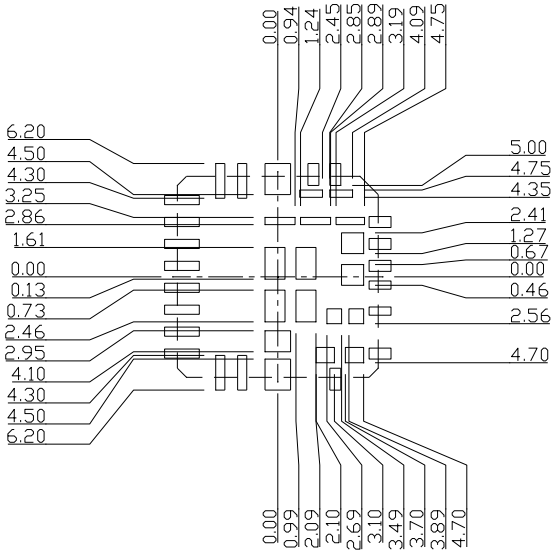
### LAND PATTERN REFERENCE:




**TYPICAL RECOMMENDED LAND PATTERN**




**STENCIL PATTERN WITH SQUIRE PADS-1**




**STENCIL PATTERN WITH SQUIRE PADS-2**

Note: All dimensions are in millimeters.

# HS2303

## 10A, High Efficiency Power Module

### REFLOW PARAMETERS:

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 34 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

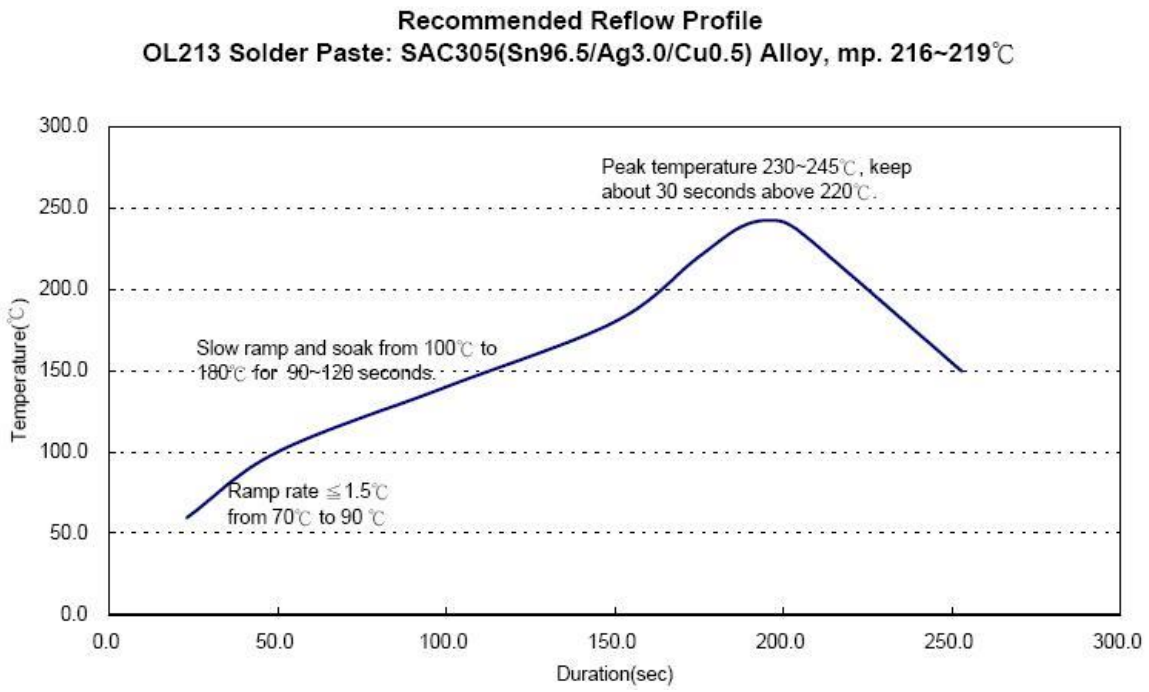



**Figure.34 Recommendation Reflow Profile**

## STORAGE AND HANDLING: (Cont.)

TABLE 3 MOISTURE CLASSIFICATION LEVEL AND FLOOR LIFE

| Level | Floor Life (out of bag) at factory ambient ≦30°C/60% RH or as stated |
|---|---|
| **1** | Unlimited at ≦30°C/85% RH |
| **2** | 1 year |
| **2a** | 4 weeks |
| **3** | 168 hours |
| **4** | 72 hours |
| **5** | 48 hours |
| **5a** | 24 hours |
| **6** | Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label. |

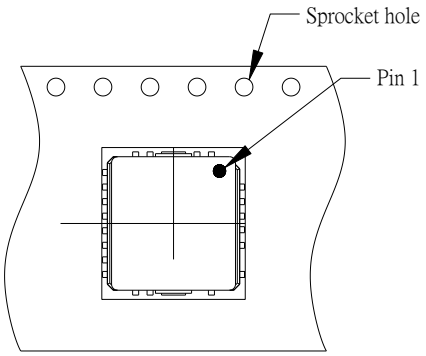
# HS2303

## 10A, High Efficiency Power Module

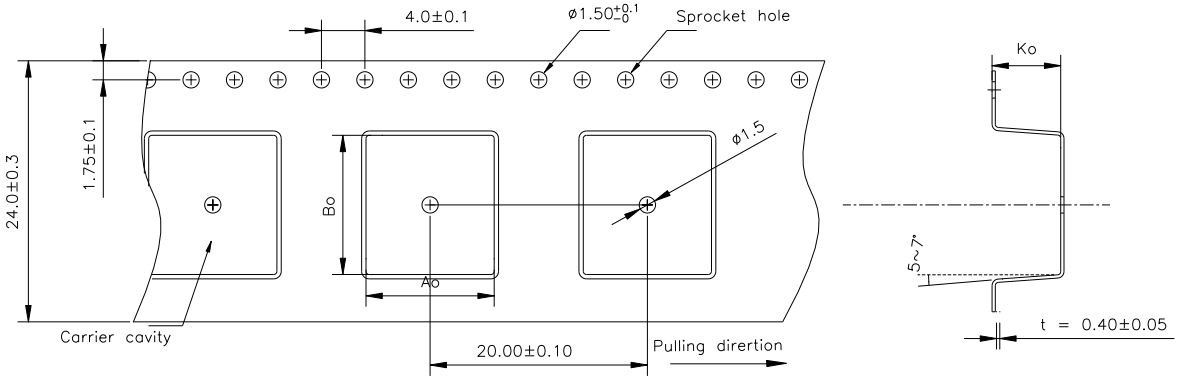
### PACKING INFORMATION:

Unit: mm

**Tape and Reel Packing**




**PACKAGE IN TAPE LOADING ORIENTATION**




**TAPE DIMENSION**

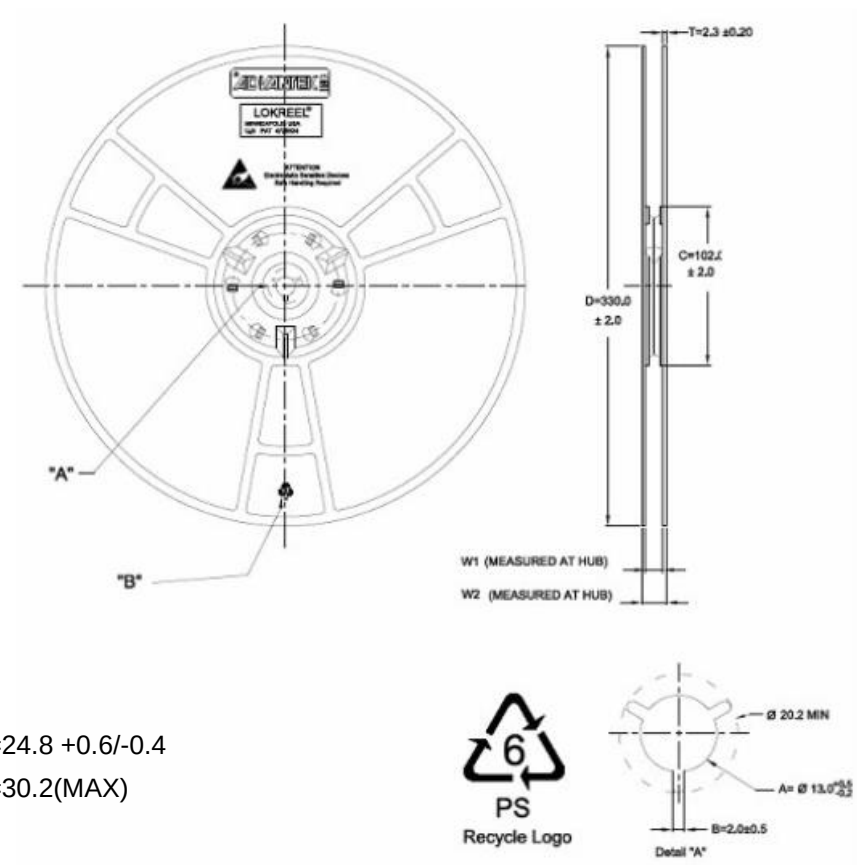
| | |
|---|---|
| A0 | 12.20 ± 0.10 |
| B0 | 12.80 ± 0.10 |
| K0 | 6.3 ± 0.10 |

# HS2303

## 10A, High Efficiency Power Module

### PACKING INFORMATION: (Cont.)

Unit: mm




W1=24.8 +0.6/-0.4

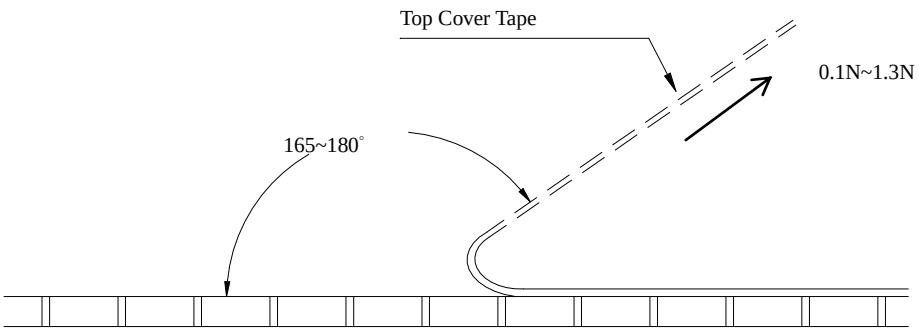
W2=30.2(MAX)

**REEL DIMENSION**

**Peel Strength of Top Cover Tape**

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



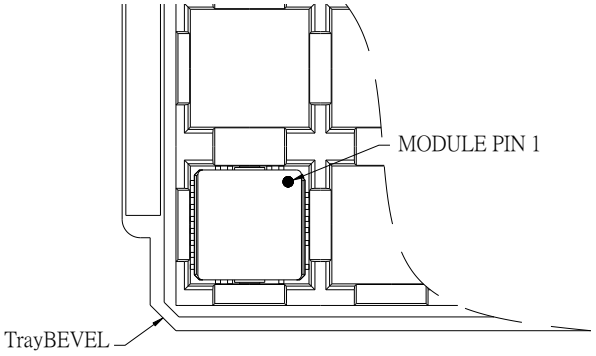
# HS2303

## 10A, High Efficiency Power Module

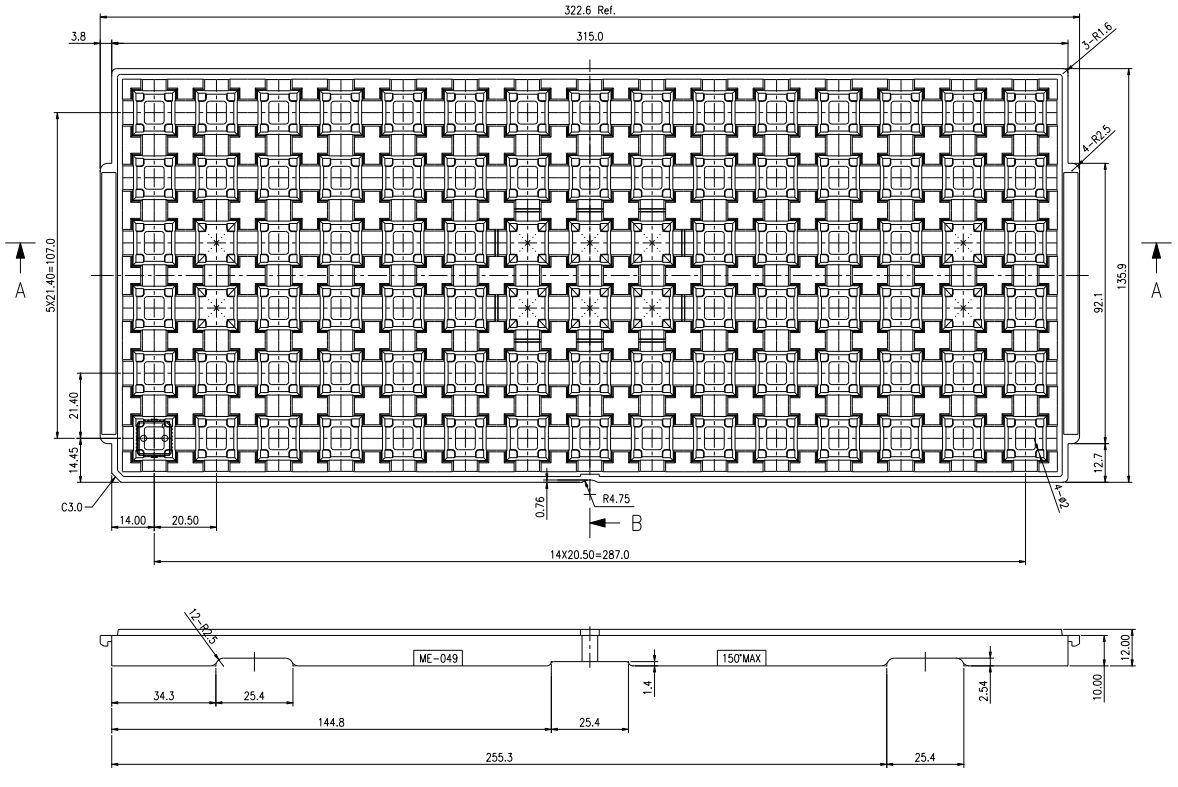
### PACKING INFORMATION: (Cont.)

Unit: mm

**Tray Packing**




**PACKAGE IN TRAY LOADING ORIENTATION**




**TRAY DIMENSION**